Table of Contents: Volume 3 (1991)

Numbers 1/2

Special Issue: Parallel Processing on VLSI Arrays
Guest Editor: Josef A. Nossek

Introduction, *Josef A. Nossek* 5

Numerical Integration of Partial Differential Equations Using Principles of Multidimensional Wave Digital Filters
Alfred Fettweis and Gunnar Nitsche 7

Signal Processing Using Cellular Neural Networks
L.O. Chua, L. Yang and K.R. Krieg 25

Nonlinear Analog Networks for Image Smoothing and Segmentation
A. Lumsdaine, J.L. Wyatt, Jr. and I.M. Elfadel 53

A Systolic Array for Nonlinear Adaptive Filtering and Pattern Recognition
J.G. McWhirter, D.S. Broomhead and T.J. Shepherd 69

Control Generation in the Design of Processor Arrays
Jürgen Teich and Lothar Thiele 77

A Sorter-Based Architecture for a Parallel Implementation of Communication Intensive Algorithms
Josef G. Krammer 93

Feedforward Architectures for Parallel Viterbi Decoding
Gerhard Fettweis and Heinrich Meyr 105

Carry-Save Architectures for High-Speed Digital Signal Processing
Tobias G. Noll 121

Number 3

Special Issue: Algorithms and Parallel VLSI Architecture
Guest Editor: Ed F. Deprettere

Editorial, *S.Y. Kung* 147

Introduction, *Ed F. Deprettere* 149

Systolic Implementations of Up/Down-dating Cholesky Factorization Using Vectorized Gram-Schmidt Pseudo Orthogonalization
S.F. Hsieh, K.J.R. Liu and K. Yao 151

A Square Root Covariance Algorithm for Constrained Recursive Least Squares Estimation
Marc Moonen and Joos Vandewalle 163

The ALPHA Language and Its Use for the Design of Systolic Arrays
Hervé Le Verge, Christophe Mauras and Patrice Quinton 173

Synthesis of ASIC Regular Arrays for Real-Time Image Processing Systems
Michaël van Swaaij, Jan Rosseel, Francky Catthoor and Hugo De Man 183

In-Place Memory Management of Algebraic Algorithms on Application Specific ICs
Ingrid Verbauwhede, Francky Catthoor, Joos Vandewalle and Hugo De Man 193

Linear Pseudo-systolic Array for Partitioned Matrix Algorithms
Jaime H. Moreno, Miguel E. Figueroa and Tomás Lang 201

Bit-Level Systolic Arrays for Modular Multiplication
Çetin K. Koç and Ching Yu Hung 215

Regular Papers

Testing and Diagnosis of FFT Arrays
A. Antola, M.G. Sami and D. Sciuto 225

A Systolic Array for Pyramidal Algorithms
Christian Lengauer and Jingling Xue 237

Number 4
Special Issue: Comuter Arithmetic
Guest Editors: Vojin G. Oklobdzija and Belle W.Y. Wei

Introduction, Vojin G. Oklobdzija and Belle W.Y. Wei 263

Improved CLA Scheme with Optimized Delay
Brian D. Lee and Vojin G. Oklobdzija 265

A Note on Designing Two-Level Carry-Skip Adders
Pak K. Chan and Martine D.F. Schlag 275

High-Performance VLSI Multiplier with a New Redundant Binary Coding
Xiaoping Huang, Belle W.Y. Wei, Honglu Chen, and Yuhai H. Mao 283

Cost-Efficient High-Radix Division
Eric M. Schwarz and Michael J. Flynn 293

Gate Array Implementation of On-Line Algorithms for Floating-Point Operations
Paul K.-G. Tu and Milos D. Ercegovac 307

Multiplication of Complex Numbers Encoded as Polynomials
Thanos Stouraitis and Alexander Skavantzos 319

New Algorithms for Reconfiguring VLSI/WSI Arrays
Theodora A. Varvarigou, Vwani P. Roychowdhury and Thomas Kailath 329

Use of Window Addressable Memories for High Speed Geometrical Analysis
Vibeke Libby 345